What is claimed is:

1. A method for forming an interconnect structure comprising:

forming a first dielectric layer over a conductive layer using chemical vapor deposition;

forming a second dielectric layer over said first dielectric layer by spin coating;

via etching said second dielectric layer and said first dielectric layer to form a via opening extending through said second dielectric layer and said first dielectric layer ;

filling said via opening with a plug material; and

trench etching said second dielectric layer and said plug material to form a trench over a lower portion of said via opening and to remove said plug material from said via opening, thereby forming a dual damascene opening.

2. The method as in claim 1, wherein each of said first dielectric layer and said second dielectric layer comprise low-k dielectric materials.

3. The method as in claim 1, wherein said plug material comprises photoresist.

4. The method as in claim 1, wherein said plug material comprises a spin-on low-k dielectric material.

5. The method as in claim 4, wherein said second dielectric layer is a low-k dielectric material that is the same as said spin-on low-k dielectric material.

6. The method as in claim 5, wherein said first dielectric layer and said spin-on low-k dielectric material have different etch rates during said trench etching.

7. The method as in claim 1, wherein said first dielectric layer and said second dielectric layer have different etch rates during said trench etching.

8. The method as in claim 1, wherein said first dielectric layer is substantially resistant to being etched during said trench etching.

9. The method as in claim 1, wherein said first dielectric layer and said second dielectric layer have an etch selectivity no less than 20:1 in said trench etching.

10. The method as in claim 1, wherein said trench etching includes at least one of H_2, N_2, A_r and O_2 as an etch gas.

11. The method as in claim 1, wherein said trench etching includes using only H_2, N_2, A_r and O_2 as etch gases.

12. The method as in claim 1, wherein said filling comprises coating said plug material over said second dielectric layer and filling said via opening, and one of polishing and etching back said plug material.

13. The method as in claim 1, further comprising forming an antireflective coating layer over said plug material and said second dielectric layer after said filling.

14. The method as in claim 1, further comprising forming a further layer over said second dielectric layer prior to said via etching and in which said via etching further comprises etching said further layer, said further layer comprising at least one of a hardmask and an anti-reflective coating.

15. The method as in claim 1, wherein said forming a first dielectric layer over a conductive layer further comprises forming an etch stop layer over said conductive layer and forming said first dielectric layer on said etch stop layer, and further comprising etching said etch stop layer after said trench etching.

16. The method as in claim 1, wherein said first dielectric layer has a dielectric constant no greater than 3.0 and is one of HBD, an oxide and an ultra low-k dielectric material having a dielectric constant less than 2.5.

17. The method as in claim 1, wherein said second dielectric layer has a dielectric constant no greater than 2.6 and is one of SiLK and porous SiLK.

18. The method as in claim 1, further comprising forming a cap layer on said first dielectric layer and in which said forming a second dielectric layer comprises forming said second dielectric layer on said cap layer and said via etch further comprises etching said cap layer.

19. The method as in claim 18, wherein said forming a cap layer comprises forming a layer of one of SiC, SiN, SiCN, SiOC and SiON.

20. The method as in claim 18, wherein said cap layer is substantially resistant to being etched during said trench etching.